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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Byung Seok Lee

Serial No.: 10/734,389

Filed: December 12, 2003

Title: METHOD FOR FORMING BIT LINE OF FLASH DEVICE

Group Art Unit: 2818

Examiner: Calvin Lee

Attorney Docket No.: 29936/39885

I hereby certify that this paper is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on **July 11, 2005.**

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AMENDMENT "B" AND RESPONSE TO FINAL OFFICIAL ACTION PURSUANT TO 37 CFR § 1.116

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

In response to the final official action dated May 12, 2005, please amend the above-identified patent application as set forth herein.

Amendments to the claims begin on page **2** of this paper.

Remarks begin on page **4** of this paper.

OK TO ENTER
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[0018] In another embodiment of the present invention, the metal hard-mask film and the bit line metal film are formed using the same metal material.

[0019] In another embodiment of the present invention, the metal hard-mask film is formed using tungsten (W) with a thickness in the range of 500 Å to 1000 Å to endure significantly as an etching barrier in the subsequent process of etching the interlayer insulation film.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The above and other objects, advantages and features of the present invention will become apparent from the following description of preferred embodiments given in conjunction with accompanying drawings, in which:

[0021] Fig. 1 is a cross-sectional view illustrating a problem due to a decrease in a pattern size between bit lines of the conventional flash device;

[0022] Fig. 2 is a lay-out diagram illustrating a problem due to a conventional method of forming a bit line of a flash device;

[0023] Figs. 3A thru 3C are cross-sectional views taken along II-II' line in Fig. 2;

[0024] Fig. 4 is a lay-out diagram showing a bit line of a flash device according to the present invention; and,

[0025] Figs. 5A to 5D are cross-sectional views taken along V-V' line in Fig. 4 for the purpose of illustrating a method for forming a bit line of a flash device according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0026] Now, embodiments of the present invention will be described in detail with reference to accompanying drawings. However, present invention is not limited to the embodiments disclosed in the following description, but can be implemented into various changes and modifications. Thus, these embodiments according to the present invention are intended to inform those skilled in the art of a scope of the present invention. The same component in the drawings is referred to the same numeral.

[0027] Shown in Fig. 4 is a lay-out diagram showing a bit line of a flash device according to the present invention. Referring to Fig. 4, a bit line B/L pattern is formed using a patterning process on a semiconductor substrate, on which word line W/L, DSL, SSL, and bit line contact plug 112 are formed. The bit line B/L of the present invention are allowed to constantly hold an interval between target bit lines by controlling conditions of a hard-mask